Abstract

A method for multiplying the frame rate of an input video signal having a line rate $f_H in$ and a frame rate $f_V in$, comprising the steps of: propagating the input video signal through just enough memory to delay the input video signal by a fraction of a frame period $1/f_V in$; speeding up the delayed video signal to a first line rate faster than $f_H in$; speeding up the input video signal to a second line rate faster than $f_H in$; supplying the speeded up video signal and the delayed speeded up video signal sequentially, one line at a time; and, writing the sequentially supplied lines into a liquid crystal display at the faster line rate, thereby writing at least some of the lines multiple times within each the frame period. A corresponding apparatus can comprise: a partial frame memory; two speedup memories; a multiplexer; and, a source of clock and control signals.